

IT IS CLAIMED:

1. A method of maintaining a compressed count of occurrences of an event that recurs during operation of a memory system, the memory system comprising a non-volatile storage section and a controller having a volatile memory, the method comprising:

copying the compressed count from the non-volatile storage section to the controller,

subsequently expanding the compressed count,

storing the expanded count in the volatile memory,

incrementing the expanded count in response to individual occurrences of the event,

determining when the incremented count matches a multiple of a first predetermined value, and

in response to the incremented count matching a multiple of said first predetermined value, updating the compressed count in the non-volatile storage section.

2. The method of claim 1, wherein the method is carried out in an electronic system including non-volatile flash memory and the recurring event includes erasure of an addressed portion of the flash memory.

3. The method of claim 2, wherein the flash memory includes said non-volatile storage section.

4. The method of claim 1, further comprising:

generating a random or pseudo-random number in response to said individual occurrences of the event;

determining when the generated random or pseudo-random number matches at least one second predetermined value, and

in response to the generated random number matching said at least one predetermined value, incrementing the compressed count in the non-volatile storage section, wherein said updating rectifies the compressed count.

5. A method of maintaining a compressed count of a number of occurrences of an event that recurs during operation of an electronic system, comprising:

incrementing a count of the number of the individual occurrences of the event,

determining when the incremented count matches a multiple of a first predetermined value, and

in response to the incremented count matching a multiple of said first predetermined value, updating a compressed count of the number of occurrences of the event within the system, wherein the compressed count is maintained in non-volatile memory.

6. The method of claim 5, wherein the incremented count is maintained in volatile memory

7. The method of claim 6, wherein the non-volatile memory is a flash memory.

8. The method of claim 7, wherein the recurring event includes erasure of an addressed portion of the flash memory.

9. The method of claim 8, wherein the system comprises a controller including a micro-processor that controls programming of data into addressed blocks of memory cells in the flash memory, reading data from addressed blocks of memory cells and erasing data from one or more of addressed blocks of memory cells at a time, and wherein the volatile memory is part of the controller.

10. The method of claim 5, further comprising:
generating a random or pseudo-random number in response to said individual occurrences of the event,
determining when the generated random or pseudo-random number matches at least one second predetermined value, and

in response to the generated random number matching said at least one predetermined value, incrementing the compressed count in the non-volatile storage section, wherein said updating rectifies the compressed count.

11. A method of maintaining a compressed count of a number of occurrences of an event that recurs during operation of a system, comprising:

determining whether a predetermined number of individual occurrences of said system event has occurred since the compressed count was updated, updating the compressed count of the number of occurrences of said system event on those occasions when the predetermined number of individual occurrences of said system event has occurred,

determining whether another event having a random or pseudo-random probability P of occurring in response to individual occurrences of said system event has occurred, and

incrementing the compressed count of the number of occurrences of said system event on those occasions when the randomly or pseudo-randomly occurring event has occurred, wherein said updating rectifies the incremented compressed count.

12. A method of operation of a system having a volatile and non-volatile memory, comprising:

maintaining a count in the volatile memory of occurrences of an event that recurs during the operation of the system,

incrementing the when the event occurs, and

in response to an indication of an improper shutdown of the system:

compressing the count, and

storing the compressed count in the non-volatile memory.

13. The method of claim 12, wherein the system is an electronic system and the non-volatile memory is a flash memory.

14. The method of claim 13, wherein the recurring event includes erasure of an addressed portion of the flash memory.

15. The method of claim 14, wherein the system comprises a controller including a micro-processor that controls programming of data into addressed blocks of memory cells in the flash memory, reading data from addressed blocks of memory cells and erasing data from one or more of addressed blocks of memory cells at a time, and wherein the volatile memory is part of the controller.

16. A non-volatile memory system, comprising:
a plurality of blocks of non-volatile memory cells wherein the cells within individual ones of the blocks are simultaneously erasable,
a controller including a micro-processor that controls programming of data into addressed blocks of memory cells, reading data from addressed blocks of memory cells and erasing data from one or more of addressed blocks of memory cells at a time,
storage provided within the plurality of blocks of memory cells that maintains first counts associated with individual ones of the memory cell blocks,
an incrementer that increases a second count in response to a corresponding addressed block being erased, and
a first comparator that causes the first count associated with the corresponding addressed blocks being erased to be updated when the second count matches a multiple of a first predetermined number.

17. The non-volatile memory system of claim 16, wherein the second count is maintained in volatile memory.

18. The non-volatile memory system of claim 17, wherein said controller comprises the volatile memory, the incrementer and the first comparator.

19. The non-volatile memory system of claim 16, further comprising:
a reserve power source, wherein, in response to an improper shut-down indication, the controller updates the first count based on the incremented value of the second count using said reserve power source.

20. The non-volatile memory system of claim 16, further comprising:

a number generator that randomly or pseudo-randomly generates a number in response to one or more of the addressed blocks being erased, and

a second comparator that causes said first count to be updated when the generated random number matches a predetermined at least one of possible numbers generated by the random number generator, wherein the updating from the first comparator rectifies the updating from the second comparator.